



PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Attn: OIPE

Haruo NISHIDA et al.

Application No.: 10/766,038

Docket No.: 118497

Filed: January 29, 2004

For: TEST CIRCUIT, INTEGRATED CIRCUIT, AND TEST METHOD

REQUEST FOR CORRECTION OF PALM RECORDS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is a photocopy of the original filing receipt on which errors have been corrected in red. These errors are being brought to the attention of the Patent and Trademark Office so that it may correct its records. A Supplemental Application Data Sheet is attached.

Respectfully submitted,

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Date: August 13, 2004

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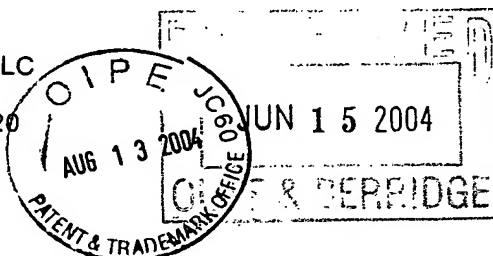


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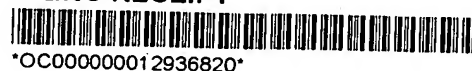
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CONFIRMATION NO. 2578

FILING RECEIPT



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Date Mailed: 06/14/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

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Assignment For Published Patent Application

SEIKO EPSON CORPORATION, Tokyo, JAPAN;

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Early Publication Request: No

Title

Test circuit, integrated circuit, and test method